



Marvell[®] JTAG Probe V User Guide




The μ Lab at your desk – debug everywhere[™]

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Document Classification: Proprietary Information

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Preface

About this Document

This document is a User Guide for the Marvell® JTAG Probe. The document is partitioned into the following two sections:

- [Section 1, Introduction](#)
- [Section 2, Marvell® Debugger XDB Support](#)

Additional Information on the Datasheet

- Rev. -(04) is the fourth edition of the of the *Marvell® JTAG Probe User Guide*.
- This reference document may include technical inaccuracies and / or typographical errors.
- Future revisions of the User Guide will correct the inaccuracies and typographical errors if any and may include updates if considered necessary.

Release Notes

Table 1: History of Document Release

Revision	Date	Description
Rev. -(01)	July 29, 2016	First Edition
Rev. -(02)	August 12, 2016	Second Edition
Rev. -(03)	August 15, 2016	Third Edition
Rev. -(04)	February 17, 2017	Fourth Edition

See [Appendix A](#) for the changes in Rev. -(04).

Feedback

Marvell® welcomes feedback on the JTAG Probe and its documentation. If there are comments and suggestions regarding this product as well as this documentation, contact a Marvell® supplier of the product. Marvell® always welcomes suggestions for additions and improvements to this documentation.

February 17, 2017

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1 Introduction

The successor to the widely used Marvell JTAG Probe III, the Marvell® JTAG Probe V (Figure 1) is supported by the Marvell® Multi Core Debugger XDB 5.7.39 and newer; as always, it is recommended that users upgrade to the latest release. This high-end and helpful - yet ultra-low cost JTAG device has been upgraded with new features. It is based on the Marvell® ARMADA™ 380, 1.6GHz and 128MB RAM.

Figure 1: Marvell® JTAG Probe V



Marvell® JTAG Probe version V supports JTAG and SWD (Serial Wire Debugging) debug interfaces, SWO (Serial Wire Output), and 4-bit TPIU. In addition to supporting SoC debug, a range of new features were added including: informative display, 16 USER I/O on 4 programmable voltage rails, frequency generator, frequency measurement, and 3 analog inputs (0 – 5V). The host connections include USB 2.0 / 3.0 high speed and Gigabit Ethernet. The Marvell® JTAG Probe version V includes a dual port Marvell® Switch. The additional GbE connection enables debugging everywhere including serial terminal support over Ethernet with the Marvell® Multi Core Debugger XDB.

The Marvell JTAG Probe webpage is accessible using port 3020.

1.1 The Marvell® JTAG Probe Connectors

1.1.1 Bezel Connectors

- **Power Jack:** 5V 1.2A minimum, center 5V, use provides international power supply
- **USB3.0:** Host connector, USB 2.0 / USB 3.0, 600mA max
- **Dual GbE:** 2 GbE switch, requires booting with external power

1.1.2 Top Connectors, Display, and Buttons

- **Display:** IP address, analog voltages, frequency input, and JTAG / Cortex reference voltage
- **Buttons:** currently unused
- **JTAG / Cortex10 / Cortex20:** connect only one of these to the target at a time; provide the JTAG and ARM specified interfaces for debugging
- **User I/O:** programmable user I/O
- **I²C / RS232:** I²C master and 3.3V TTL level serial ports, accessible through Marvell® Debugger XDB
- **Analog In:** 3 analog inputs, measure 0 – 5V, ~1% accuracy
- Use mating connectors or jumper wire cables for 2.54mm (or 0.1")

1.1.3 User I/O (view left to right, top to bottom, notch marked in grey)

v1	1.3	1.2	1.1	1.0	GND	GND	3.3V	v3	3.3	3.2	3.1	3.0	GND	GND	3.3V
v2	2.3	2.2	2.1	2.0	GND	GND	3.3V	v4	4.3	4.2	4.1	4.0	GND	GND	3.3V

- Connectors:
 - o 2x8 pins, 0.1" pitch
 - o Molex 90130 – 1216
- Mating Connector:
 - o Cable: Amphenol FCI: 71600 – 016LF
 - o Solder: Amphenol FCI: 609 – 2272-ND
- **V1 / V2 / V3 / V4:** Individually user programmable voltage level, also user I/O voltage level, up to 50mA
 - o Used for user I/O voltage level
 - o Up to 50mA
 - o 1.2V – 3.3V
- **1.0 – 4.3:** User I/O, 4 banks, 4 I/O each
 - o 1.0 & 3.0: Supports 1KHz – 100MHz frequency counter
 - o 2.0 & 4.0: Supports 50MHz/n frequency output, if n == 0 frequency output is disabled
- **GND:** Marvell® JTAG Probe ground
- **3.3V:** Internal 3.3V voltage rail, 100mA – 400mA shared (with external power supply)

1.1.4 I²C and RS232 (view left to right)

SCL	SDA	GND	V _{SRC}	NC	TX	GND	RX
-----	-----	-----	------------------	----	----	-----	----

- Used Connector:
 - o 1x8 pins, 0.1" pitch
 - o Molex 90136 – 1208
- Mating Connector:
 - o Cable: Molex 90156 – 0148 + insert
 - o Solder: Amphenol FCI: 68685 – 308LF
- **SCL/SDA:** I²C signals
- **V_{I2C}:** Input, reference voltage for I²C level, used to drive I²C level shifter
- **RX / TX:** 3.3V TTL level UART
- **Support:** Supported by Marvell® debugger XDB

1.1.5 Analog In (view left to right)

GND	AN3	AN2	AN1
-----	-----	-----	-----

- Used Connector:
 - o 1x4 pins, 0.1"pitch
 - o Molex 90136 – 1204
- Mating Connector:
 - o Cable: Molex 90156 – 0148 + insert
 - o Solder: Amphenol FCI: 68685 – 304LF
- 3 Analog inputs, 0 – 5V, see display and in XDB

1.2 Electrical Specification

Table 2 shows the Marvell® JTAG Probe electrical specification.

Table 2: Marvell® JTAG Probe Electrical Specification

Feature	MJP-V
Power Consumption USB	5V, 450 – 600mA max; LEGAL DISCLAIMER: Marvell does not warrant against any damage to your equipment.
Power Consumption external	5V, 600 – 900mA
JTAG, Cortex-20, Cortex-10	1.2 – 3.3V (self-adapting) < 1mA
User I/O	1.1 – 3.6V
User voltage rail	0.0 – 4.0V, max 30mA
3.3V rail	100mA (USB power) – 400mA (external power)



Note

The power rails are not current limited; drawing too much power may damage the device permanently.



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Marvell® Debugger XDB Support

Up to XDB 5.7.56, the debugger connection string has to be changed to "MJPTCP:<ipaddr>"; the IP address is showed on the MJP-V display. Newer debuggers support the connection string "USB:" and check for MJP-V using the default Ethernet over USB IP address.

The XDB integrated terminal plug-in VT100 supports MJP as a serial com port which also enables serial port over Ethernet. Normal RS232 ports are opened by using "VT100 SETCOM COMn:115200", the Marvell® JTAG Probe RS232 port can be used using "VT100 SETCOM MJP:115200".

Using "TCI HELP" will display additional command support I²C and user I/O functions. [Table 3](#) shows the list of external connectors.

Table 3: List of external Connectors¹

Feature	Description
USB 2.0 / 3.0	USB 2.0 / 3.0 high speed host connection
<i>Gigabit Ethernet</i>	Gigabit Ethernet (GbE) connection with an dual port switch
<i>External Power</i>	Enables GbE switch and provides better power level for User I/O
<i>Display</i>	Informative display (e.g. IP address, analog input)
JTAG	20 pin 0.1" pitch JTAG cable
<i>CRTX-10</i>	0.05" pitch, 10 pin connector, ~1/8 of the board size requirements than JTAG
<i>CRTX-20</i>	0.05" pitch, 20 pin connectors, ¼ of the board size requirements than JTAG; added 4-bit TPIU support
<i>USER I/O</i>	4 I/O banks - Individually programmable 0 – 4V, up to 30 mA - 4 user I/O per bank - GND - 3.3V, 100mA - 400mA Additional User I/O features - I/O bank 1 & 2, pin 0: frequency measurements 1KHz – 100MHz - IO bank 3 & 4, pin 0: frequency out, 50MHz/n (n: 1 – 65535)
<i>RS232</i>	3.3V TTL level RS232
<i>I²C</i>	Dedicated I ² C channel from external devices
<i>3 analog In</i>	0 – 5V 8bit (±1 bit) accurate; values show on display ~ 20 minute history, 50 measurements / sec

1. Bold / Italic implies new features

Table 4 shows the List of MJP-V features.

Table 4: List of MJP-V Features¹

Feature	Description
XDB Support	XDB 5.7.39 and newer
15Hz – 60MHz TCK	Wide range of support for TCK and SCLK from 15Hz to 60MHz
Self-adaptive V_{tref}	1.2 - 3.3V V_{tref} support, active voltage control Measure SRST, TRST, V_{tref} (JTAG, CRTX-10, CRTX-20)
JTAG SWD / SWO / TPIU	JTAG 1149.1 standard ARM specific Serial Wire Debug (SWD) with SWO and 4-bit TPIU (up to 100 MHz DDR)
Webpage	Device Web Server on port 3020 (<a href="http://<ipaddr>:3020">http://<ipaddr>:3020)
SPI programming	Supports direct external SPI programming
User add-on	User can provide additional add-on services for the MJP-V board

1. ***Bold/Italic***: features in MJP-V that are additional to the MJP-III

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A Appendix

A.1 Revision History

This section tracks the changes when a new document revision is released.

Table 5: History of Changes

Rev #	Date	Description
01	July 29, 2016	Draft version
02	August 12, 2016	Draft version
03	August 15, 2016	Released version.
04	February 17, 2017	Updated Figure 1 on page 7 . 256MB RAM is updated to 128MB RAM in Section 1 . The I/O table is reorganized in Section 1.1.3 .

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