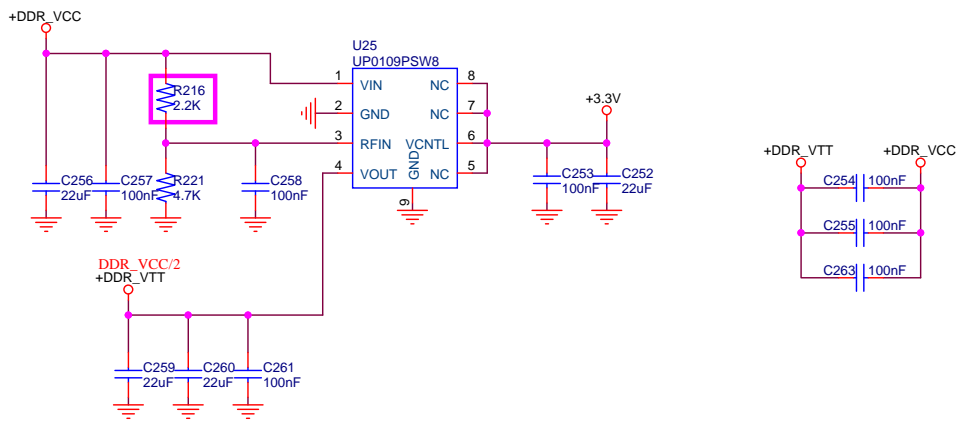
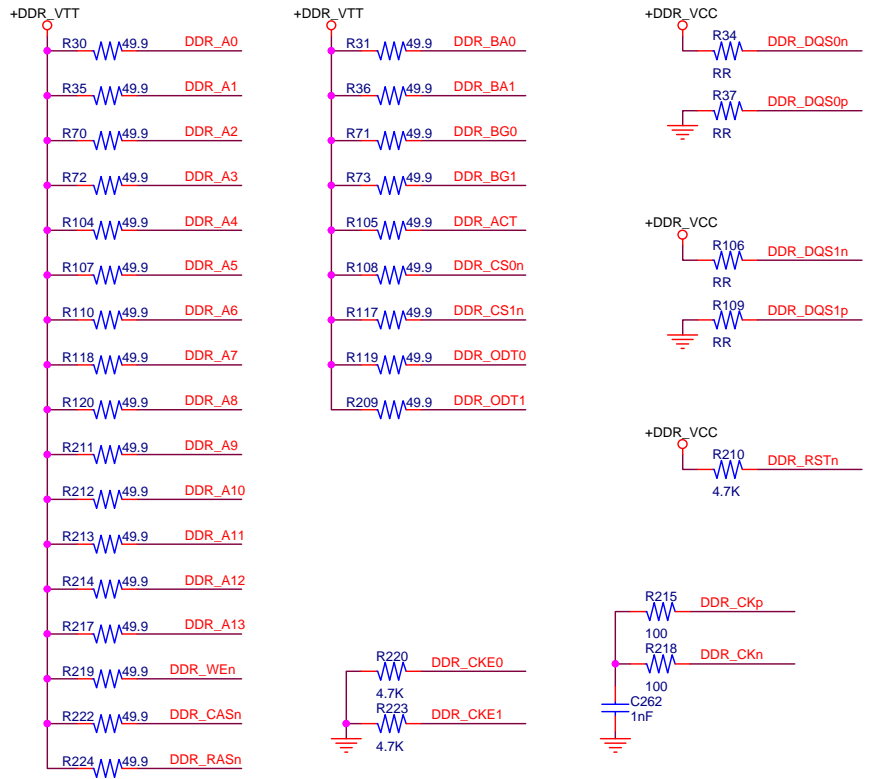
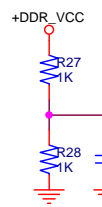
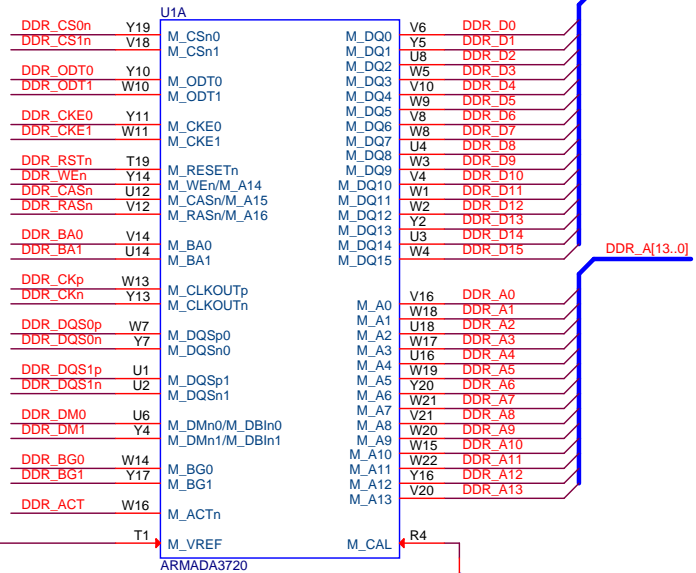


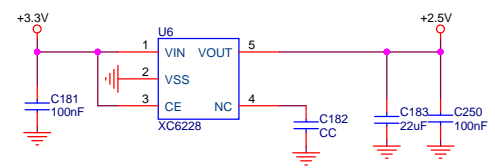
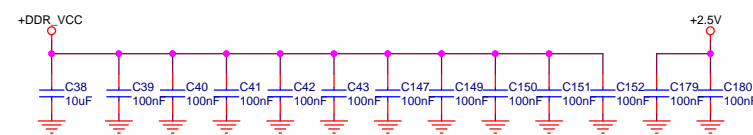
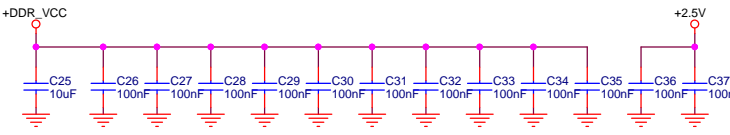
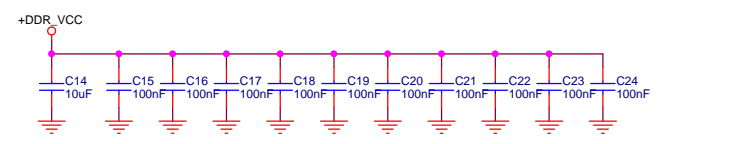
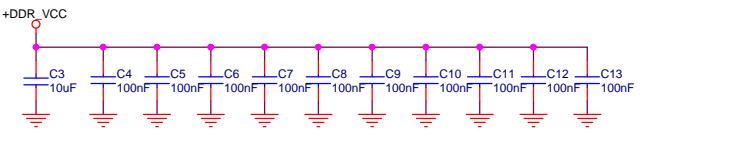
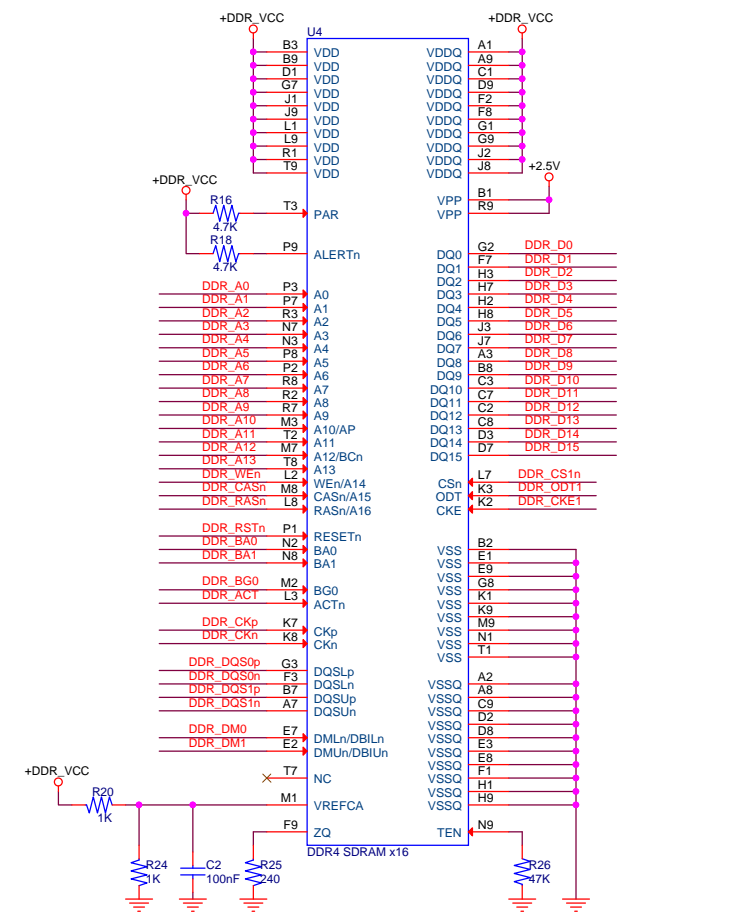
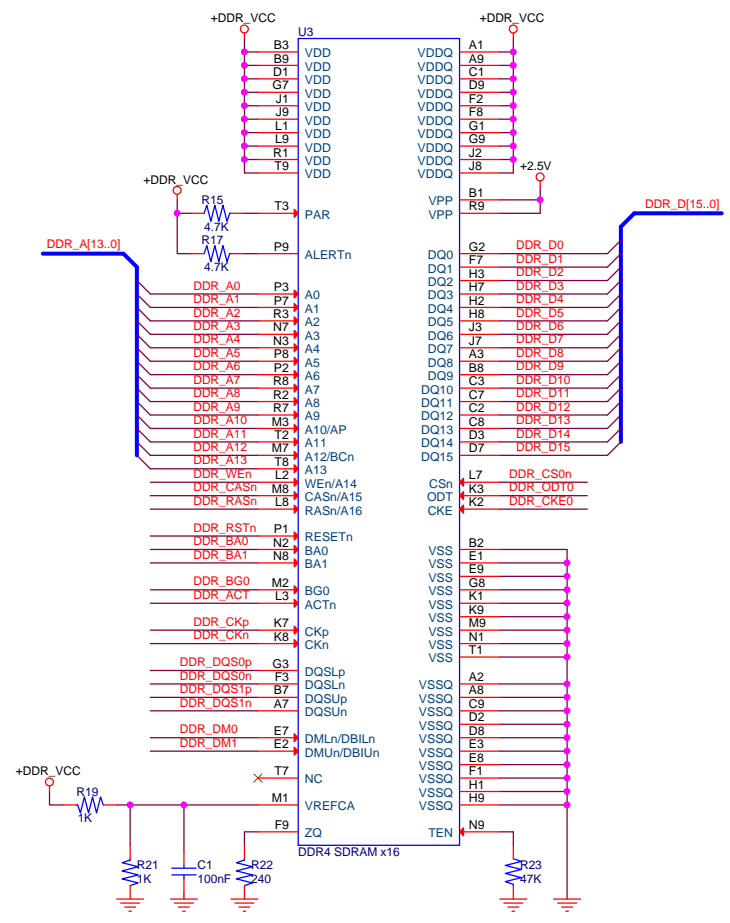
P2: DDR4

DDR_A[13..0]	DDR_A[13..0]
DDR_D[15..0]	DDR_D[15..0]
DDR_WEn	DDR_WEn
DDR_CASn	DDR_CASn
DDR_RASn	DDR_RASn
DDR_RSTn	DDR_RSTn
DDR_BA0	DDR_BA0
DDR_BA1	DDR_BA1
DDR_BG0	DDR_BG0
DDR_ACT	DDR_ACT
DDR_CkP	DDR_CkP
DDR_CkN	DDR_CkN
DDR_DQS0p	DDR_DQS0p
DDR_DQS0n	DDR_DQS0n
DDR_DQS1p	DDR_DQS1p
DDR_DQS1n	DDR_DQS1n
DDR_DM0	DDR_DM0
DDR_DM1	DDR_DM1
DDR_CS0n	DDR_CS0n
DDR_ODT0	DDR_ODT0
DDR_CKE0	DDR_CKE0
DDR_CS1n	DDR_CS1n
DDR_ODT1	DDR_ODT1
DDR_CKE1	DDR_CKE1



P1: DDR

DDR_A[13..0]	DDR_A[13..0]
DDR_D[15..0]	DDR_D[15..0]
DDR_WEn	DDR_WEn
DDR_CASn	DDR_CASn
DDR_RASn	DDR_RASn
DDR_RSTn	DDR_RSTn
DDR_BA0	DDR_BA0
DDR_BA1	DDR_BA1
DDR_BG0	DDR_BG0
DDR_ACT	DDR_ACT
DDR_CkP	DDR_CkP
DDR_CkN	DDR_CkN
DDR_DQS0p	DDR_DQS0p
DDR_DQS0n	DDR_DQS0n
DDR_DQS1p	DDR_DQS1p
DDR_DQS1n	DDR_DQS1n
DDR_DM0	DDR_DM0
DDR_DM1	DDR_DM1
DDR_CS0n	DDR_CS0n
DDR_ODT0	DDR_ODT0
DDR_CKE0	DDR_CKE0
DDR_CS1n	DDR_CS1n
DDR_ODT1	DDR_ODT1
DDR_CKE1	DDR_CKE1



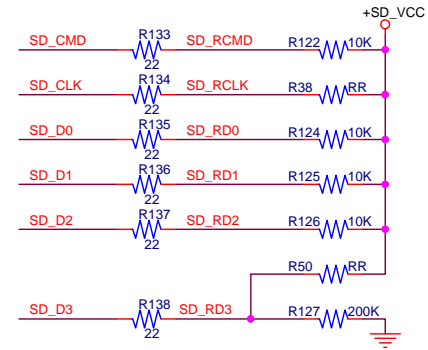
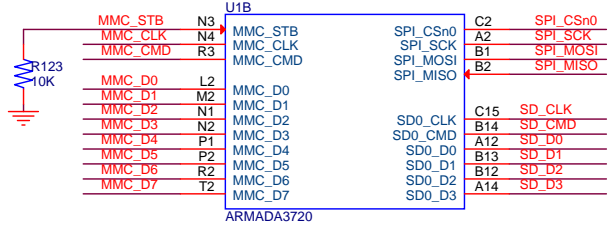
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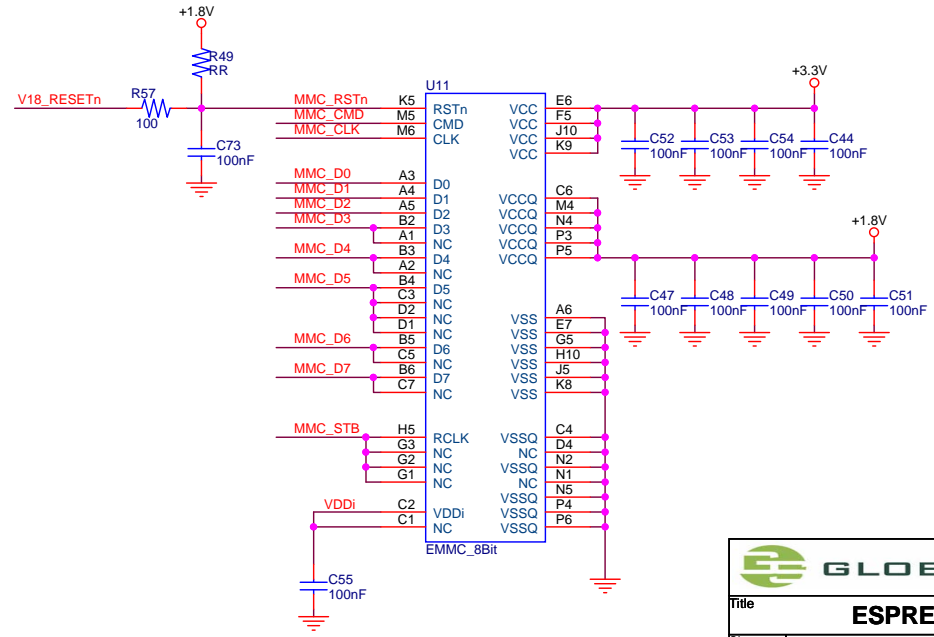
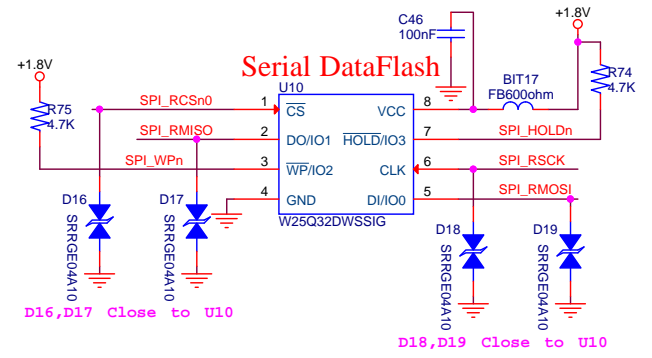
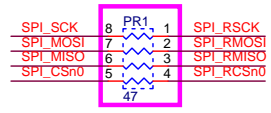
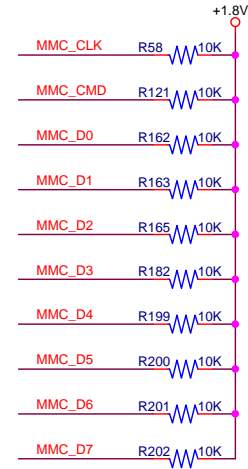
Size	Document Number	Rev
A4	02-DDR4_16x2	V7-3-3

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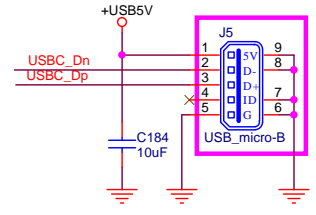
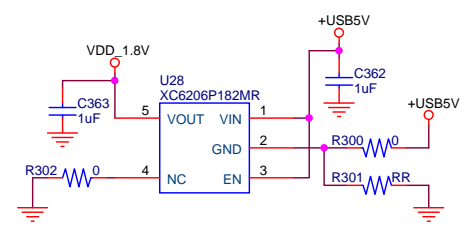
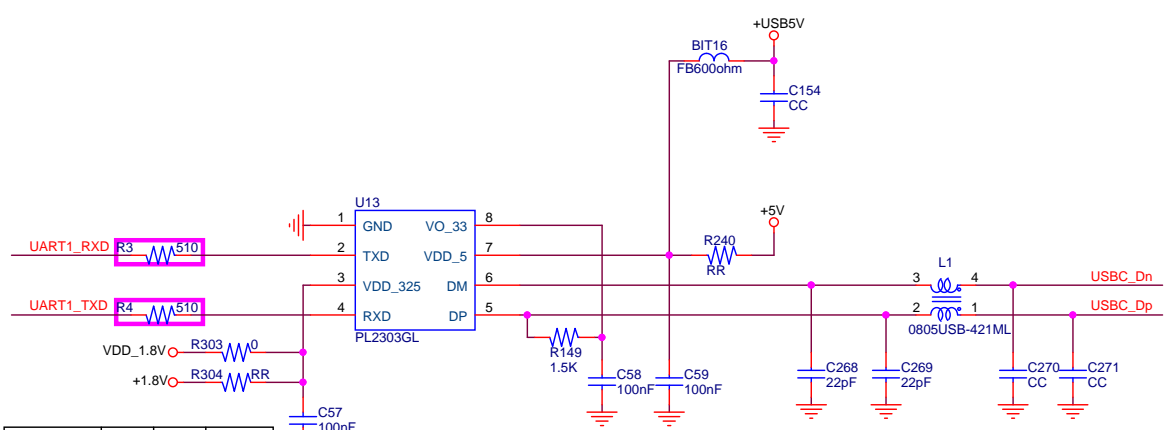
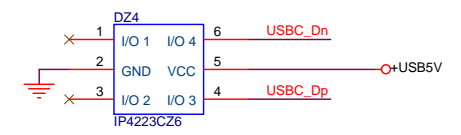
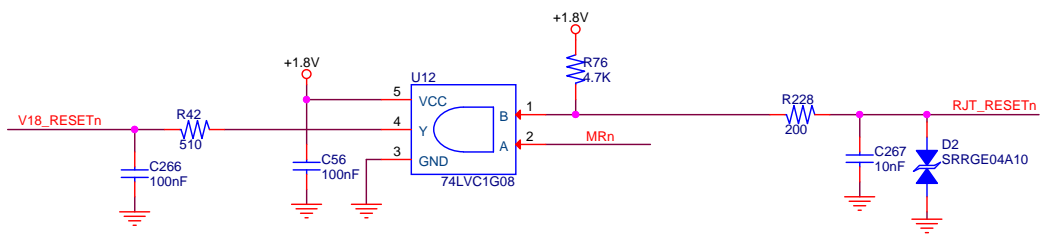
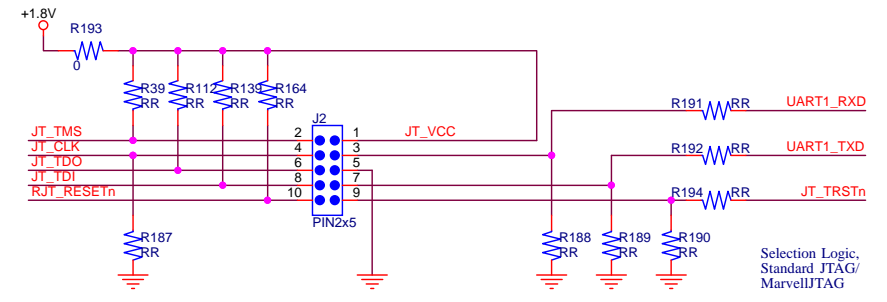
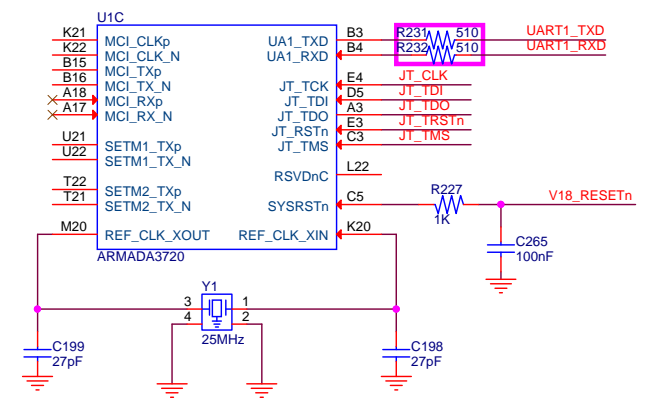
- P4: JTAG
P8: GPIO
P9: Ethernet_SW
P11: IO
V18_RESETEn <- V18_RESETEn
- P8: GPIO
SPI_HOLDn <- SPI_HOLDn
SPI_WPn <- SPI_WPn
SD_CDZ <- SD_CDZ
- P11: IO
MMC_CLK <- MMC_CLK
MMC_CMD <- MMC_CMD
MMC_D0 <- MMC_D0
MMC_D1 <- MMC_D1
MMC_D2 <- MMC_D2
MMC_D3 <- MMC_D3
MMC_D4 <- MMC_D4
MMC_D5 <- MMC_D5
MMC_D6 <- MMC_D6
MMC_D7 <- MMC_D7
SPI_CS0 <- SPI_CS0
SPI_SCK <- SPI_SCK
SPI_MOSI <- SPI_MOSI
SPI_MISO <- SPI_MISO



If required SD card autodetection - SD_RD3 should be PD via 200k



P3:MEM
P8:GPIO
P9:Ethernet_SW
P11:IO
V18_RESETEn ← V18_RESETEn
MRn ← MRn
P13:DC-DC



U13	R303	R304	U28
PL2303SA	RR	0	不上件
PL2303GL	0	RR	上件

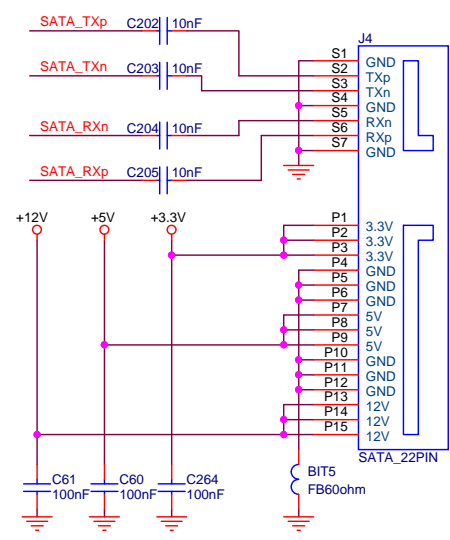
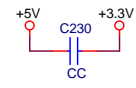
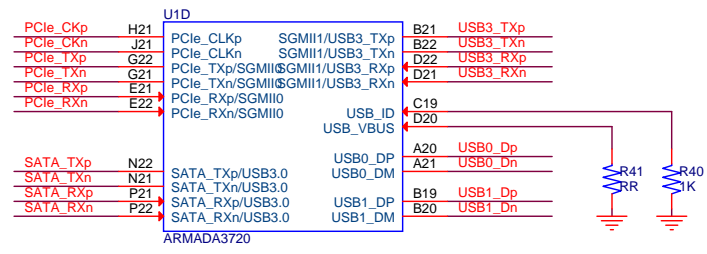
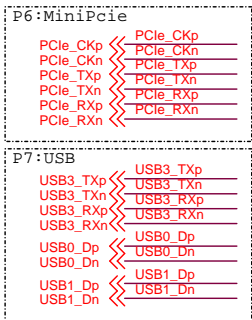
U28	R300	R301	R302
MT7110DSBR	RR	0	RR
XC6206P182MR	0	RR	0

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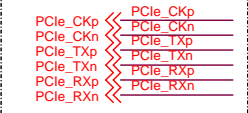
Title: **ESPRESSObin**

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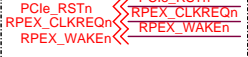
P5: INTERFACE



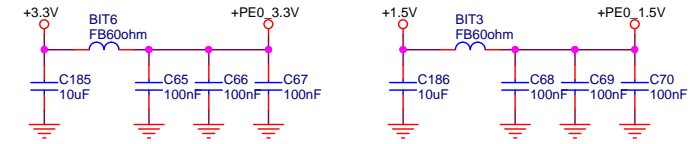
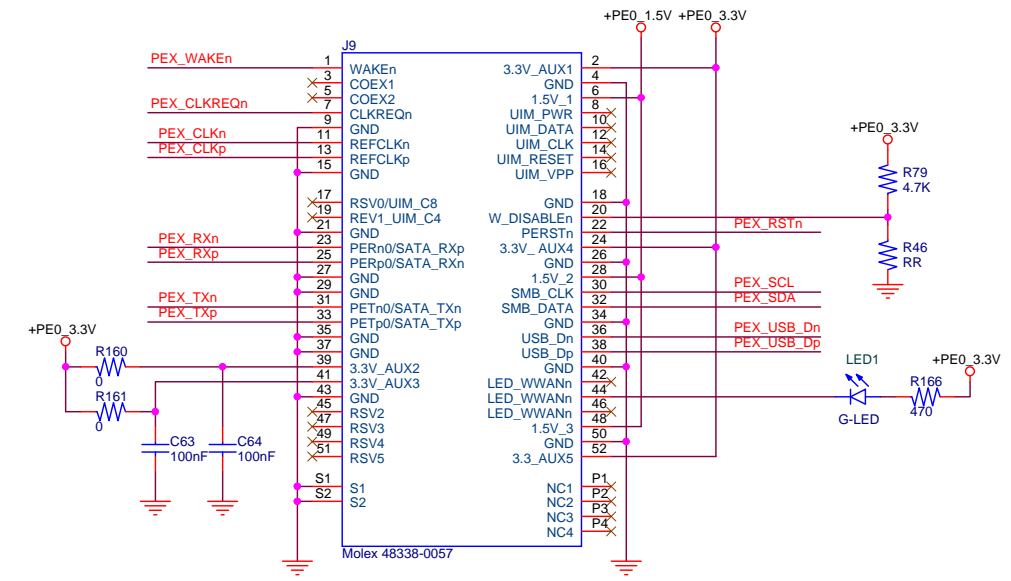
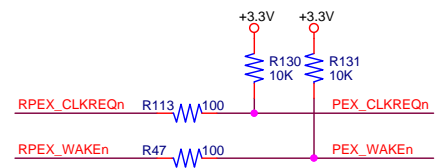
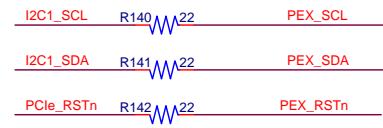
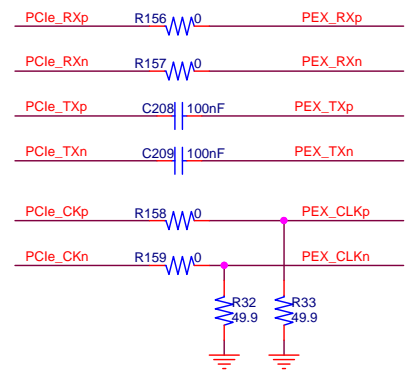
P7: USB



P8: GPIO



P8: GPIO



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Title: **ESPRESSObin**

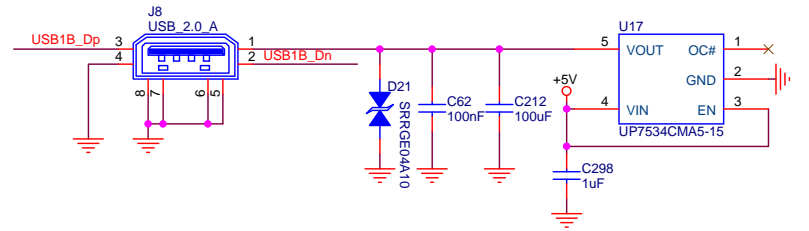
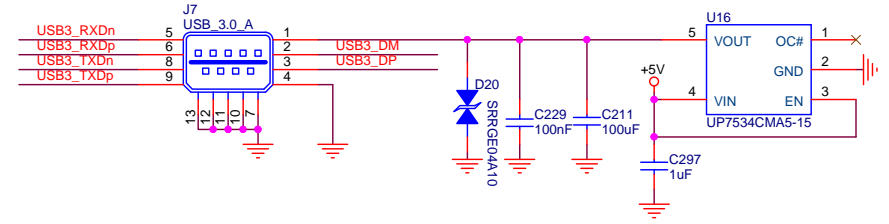
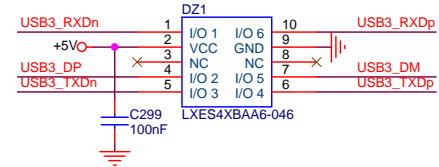
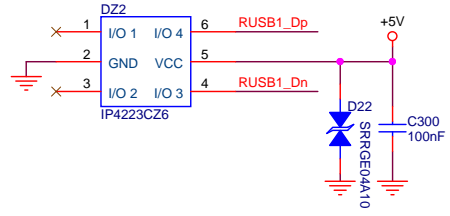
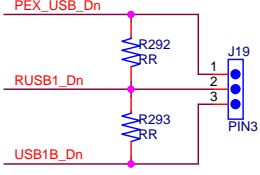
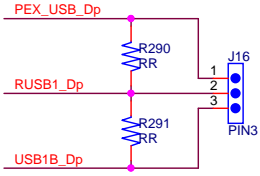
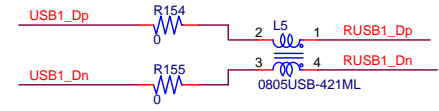
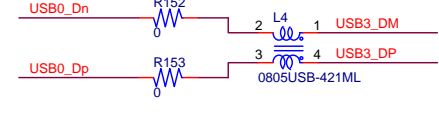
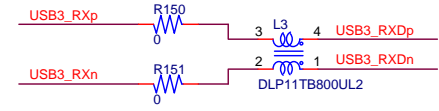
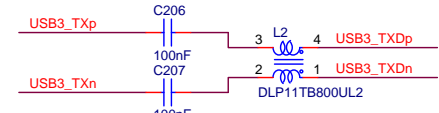
Size: A4	Document Number: 06-MiniPcie	Rev: V7-3-3
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P5: INTERFACE

USB3_TXp ↔ USB3_TXp
 USB3_TXn ↔ USB3_TXn
 USB3_RXp ↔ USB3_RXp
 USB3_RXn ↔ USB3_RXn
 USB0_Dp ↔ USB0_Dp
 USB0_Dn ↔ USB0_Dn
 USB1_Dp ↔ USB1_Dp
 USB1_Dn ↔ USB1_Dn

P6: MiniPcie

PEX_USB_Dp ↔ PEX_USB_Dp
 PEX_USB_Dn ↔ PEX_USB_Dn



P3: MEM
P4: JTAG
P9: Ethernet_SW
P11: IO
V18_RESEtN << V18_RESEtN

P3: MEM
SPI_HOLDn << SPI_HOLDn
SPI_WPn << SPI_WPn
SD_CDZ << SD_CDZ

P6: MiniPcie
PCle_RSTn << PCle_RSTn
RPEX_CLKREQn << RPEX_CLKREQn
RPEX_WAKEn << RPEX_WAKEn

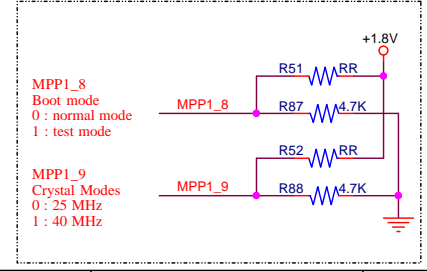
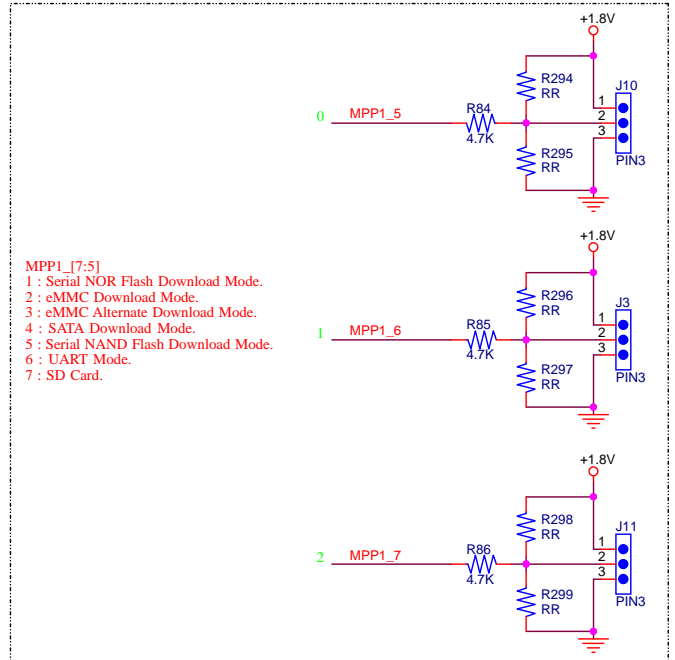
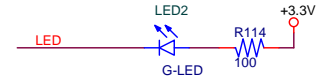
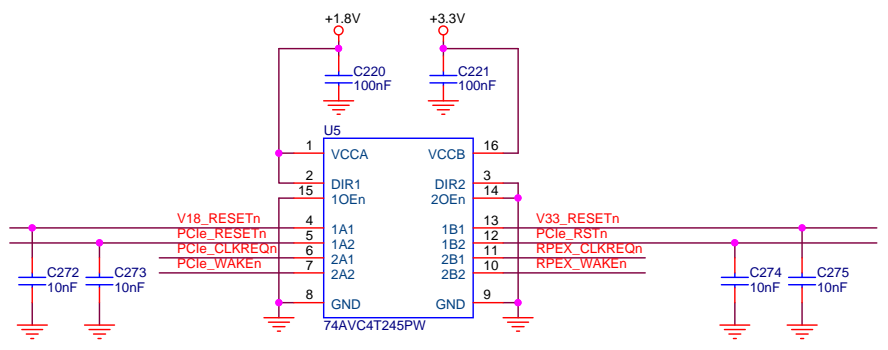
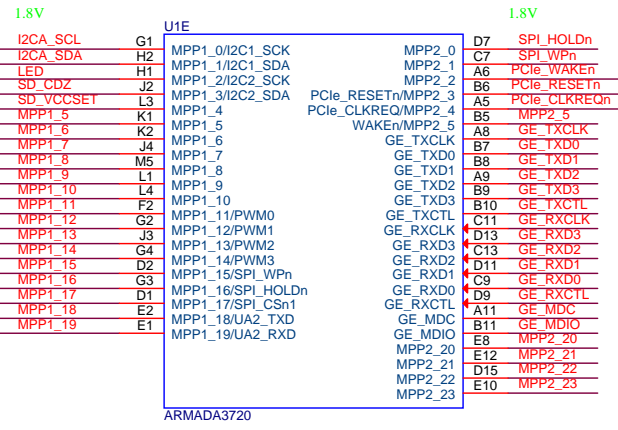
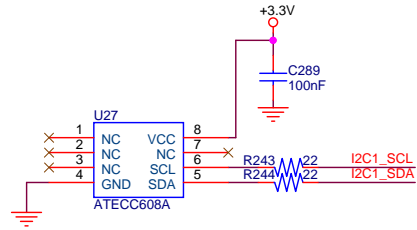
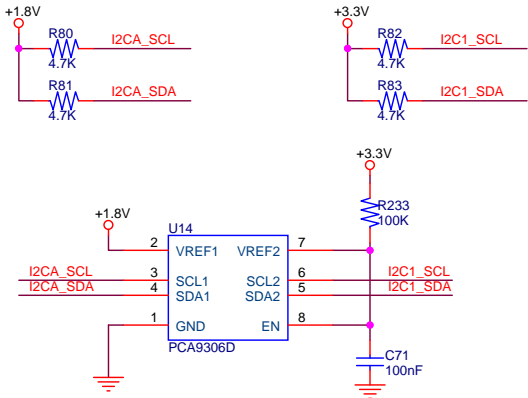
P6: MiniPcie
P11: IO
I2C1_SDA << I2C1_SDA
I2C1_SCL << I2C1_SCL

P9: Ethernet_SW
GE_TXCLK << GE_TXCLK
GE_TXD0 << GE_TXD0
GE_TXD1 << GE_TXD1
GE_TXD2 << GE_TXD2
GE_TXD3 << GE_TXD3
GE_TXCTL << GE_TXCTL
GE_RXCLK << GE_RXCLK
GE_RXD3 << GE_RXD3
GE_RXD2 << GE_RXD2
GE_RXD1 << GE_RXD1
GE_RXD0 << GE_RXD0
GE_RXCTL << GE_RXCTL
GE_MDC << GE_MDC
GE_MDIO << GE_MDIO

P9: Ethernet_SW
P11: IO
MPP2_23 << MPP2_23

P11: IO
MPP1_5 << MPP1_5
MPP1_6 << MPP1_6
MPP1_7 << MPP1_7
MPP1_8 << MPP1_8
MPP1_9 << MPP1_9
MPP1_10 << MPP1_10
MPP1_11 << MPP1_11
MPP1_12 << MPP1_12
MPP1_13 << MPP1_13
MPP1_14 << MPP1_14
MPP1_15 << MPP1_15
MPP1_16 << MPP1_16
MPP1_17 << MPP1_17
MPP1_18 << MPP1_18
MPP1_19 << MPP1_19
MPP2_5 << MPP2_5
MPP2_20 << MPP2_20
MPP2_21 << MPP2_21
MPP2_22 << MPP2_22
I2CA_SCL << I2CA_SCL
I2CA_SDA << I2CA_SDA
V33_RESEtN << V33_RESEtN

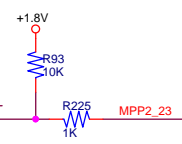
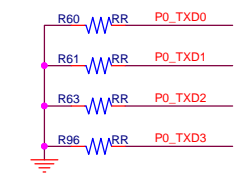
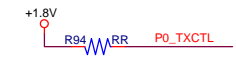
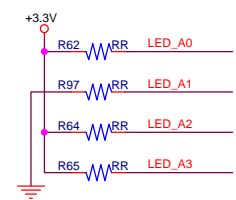
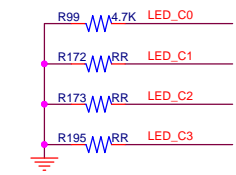
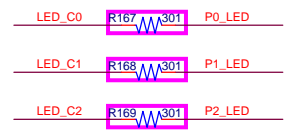
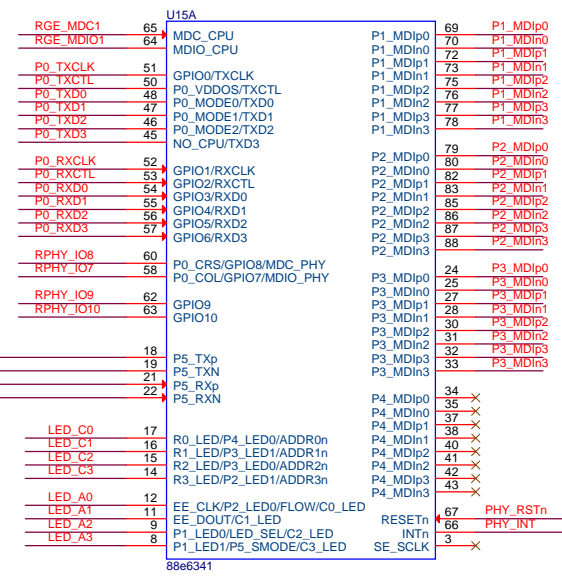
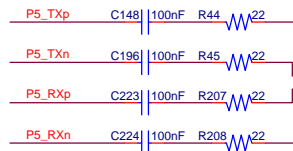
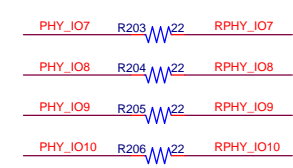
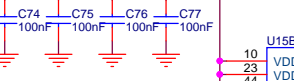
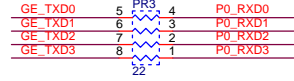
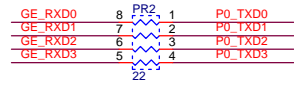
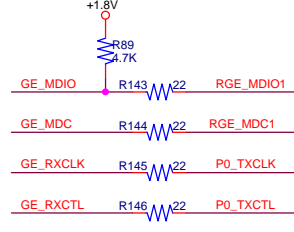
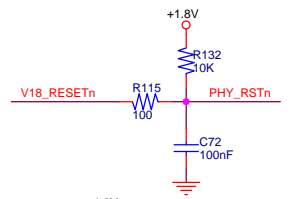
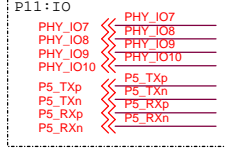
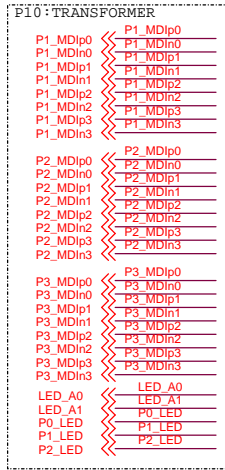
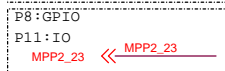
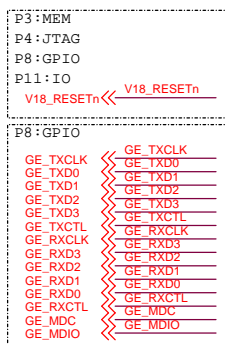
P13: DC-DC
SD_VCCSET << SD_VCCSET



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LED_C[3:0]
ADDR[3:0]

LED_A0 :
0 = Disable flow control on all ports
1 = Enable advertisement of full-duplex flow control on all PHYs and enable " forced cdli s' on" f1 w control on all half duplex por

LED_A2 :
0 = Link/Activity w/ Separate Speed LED
1 = Link/Activity w/ Speed by 3 Color

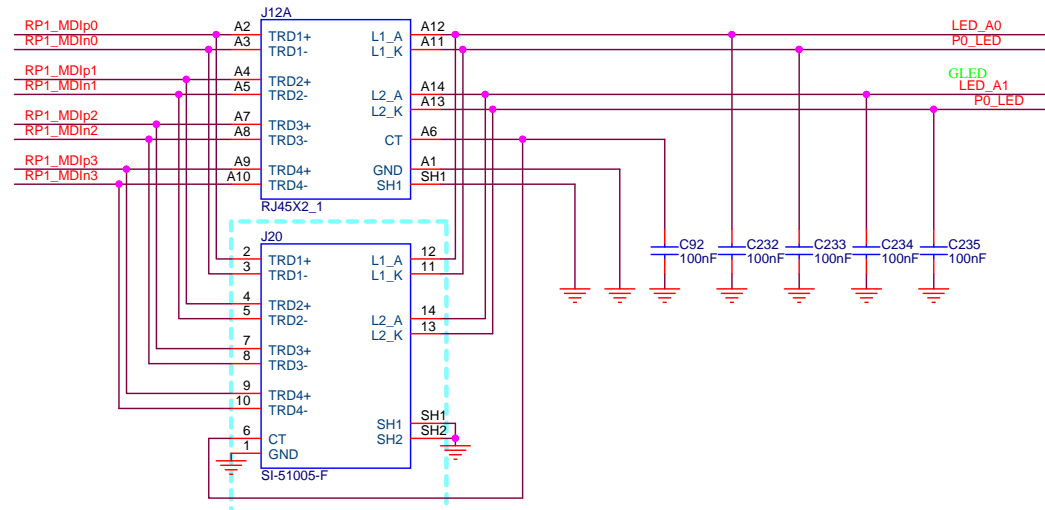
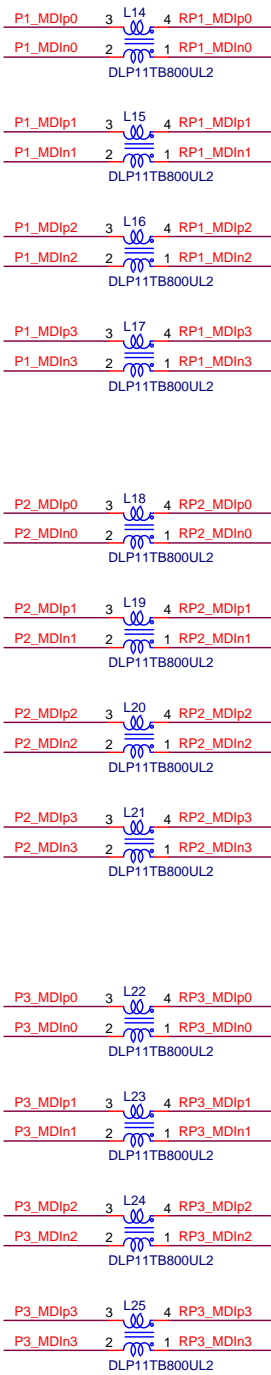
LED_A3 :
0 = 2.5Gbps Operation.
1 = SGMII/1000X Operation base on the whether PHY is detected connecting to P5 (see PHYDetect bit 0x0 bit[12]).

P0_TXLCTL_P0_VDDO
0 = The P0_VDDO pins are powered by 1.8/3.3 volts
1 = The P0_VDDO pins are powered by 2.5 volts

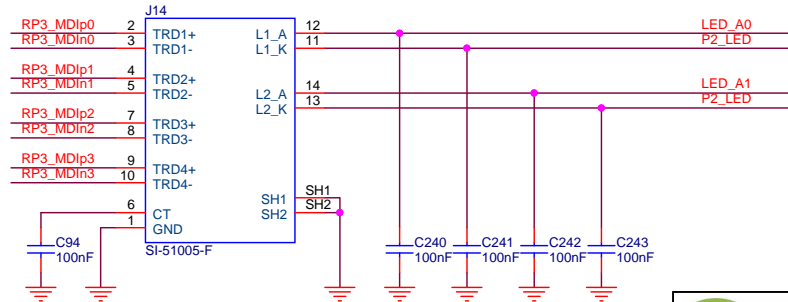
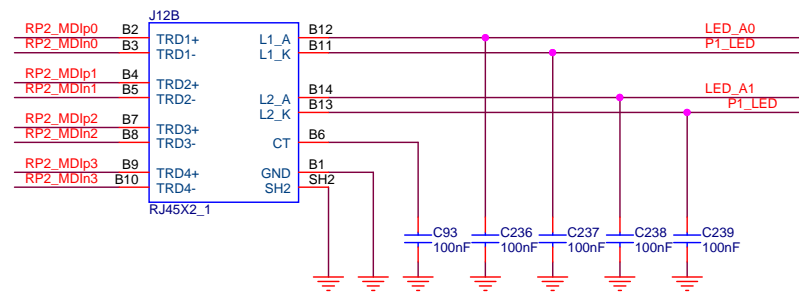
P0_TXD[2:0] P0_MODE[2:0]
0x0 = Full Duplex Only MII PHY Mode
0x1 = MII PHY mode w/output MII CLKs3 at 2.5, 25 or 50 MHz
0x2 = MII MAC mode w/input MII CLKs
0x3 = Reserved for future use
0x4 = RMI PHY mode w/output P0_OUTCLK at 50 MHz
0x5 = RMI MAC mode winput P0_OUTCLKs at 50 MHz
0x6 = Port disabled (with its pins tri-stated)
0x7 = RGMII mode
P0_TXD3
0 = CPU is attached
1 = No CPU is attached

P9: Ethernet_SW

P1_MDlp0	P1_MDlp0
P1_MDln0	P1_MDln0
P1_MDlp1	P1_MDlp1
P1_MDln1	P1_MDln1
P1_MDlp2	P1_MDlp2
P1_MDln2	P1_MDln2
P1_MDlp3	P1_MDlp3
P1_MDln3	P1_MDln3
P2_MDlp0	P2_MDlp0
P2_MDln0	P2_MDln0
P2_MDlp1	P2_MDlp1
P2_MDln1	P2_MDln1
P2_MDlp2	P2_MDlp2
P2_MDln2	P2_MDln2
P2_MDlp3	P2_MDlp3
P2_MDln3	P2_MDln3
P3_MDlp0	P3_MDlp0
P3_MDln0	P3_MDln0
P3_MDlp1	P3_MDlp1
P3_MDln1	P3_MDln1
P3_MDlp2	P3_MDlp2
P3_MDln2	P3_MDln2
P3_MDlp3	P3_MDlp3
P3_MDln3	P3_MDln3
LED_A0	LED_A0
LED_A1	LED_A1
P0_LED	P0_LED
P1_LED	P1_LED
P2_LED	P2_LED



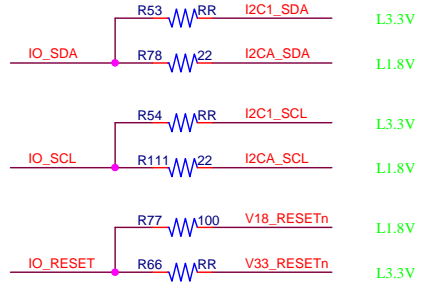
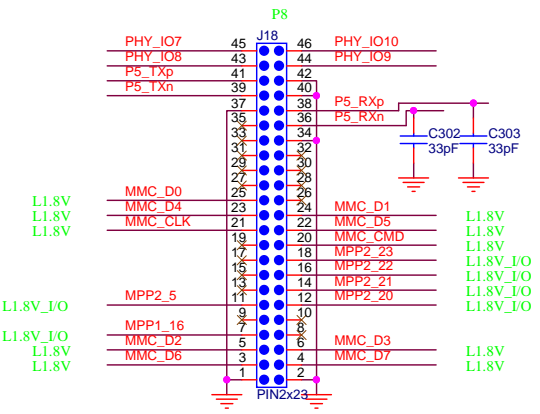
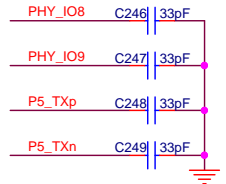
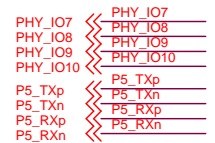
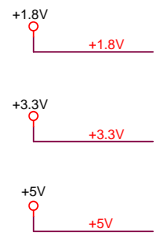
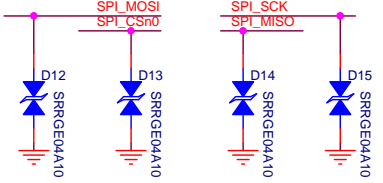
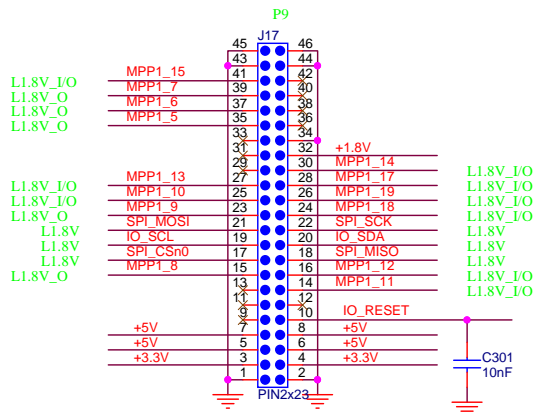
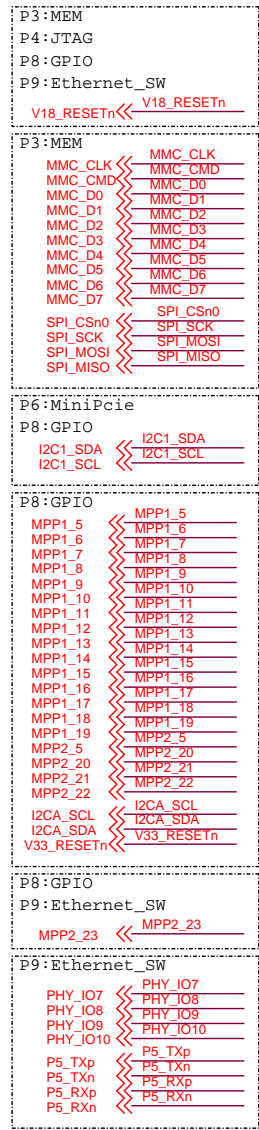
J20 for option



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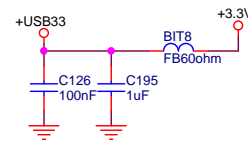
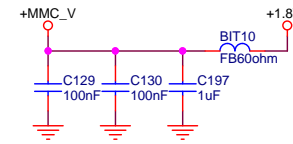
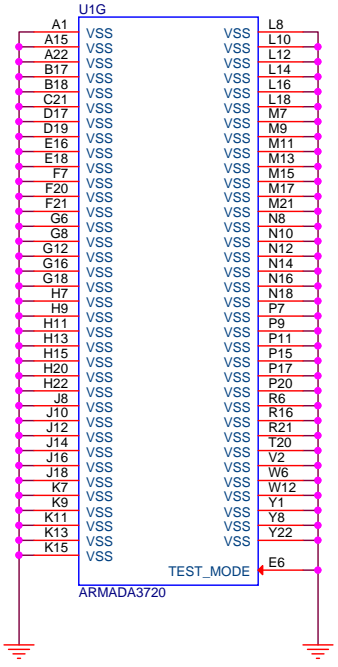
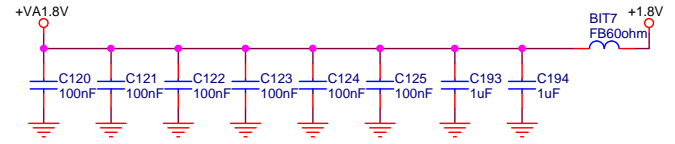
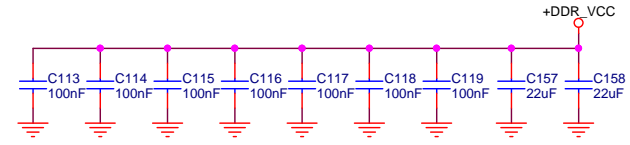
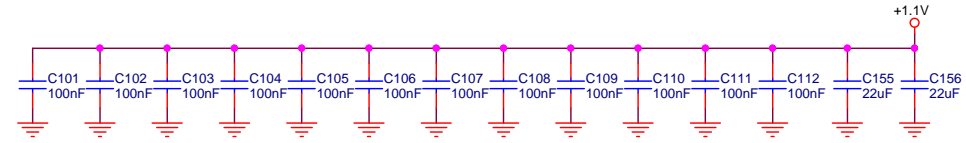
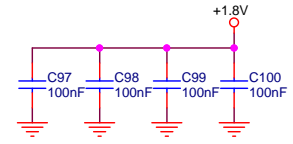
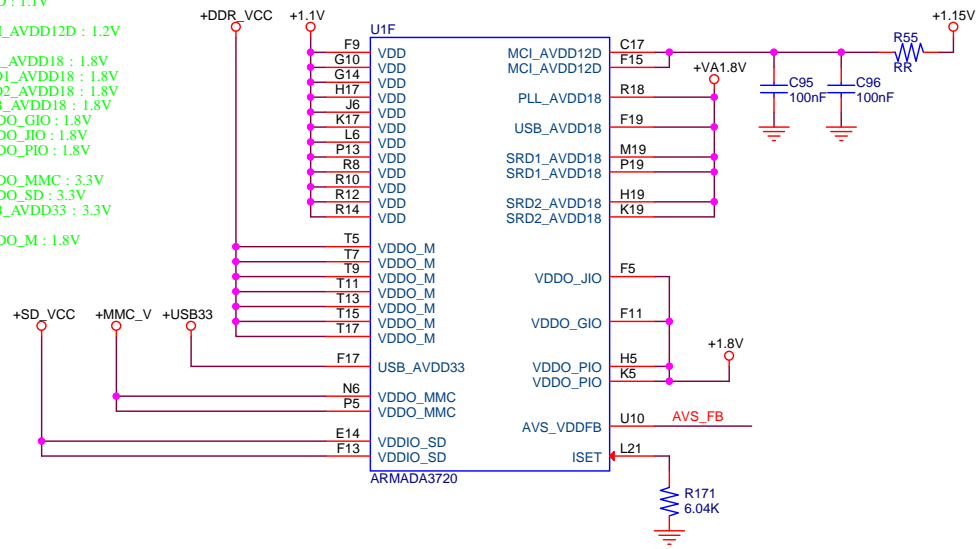
Title: **ESPRESSObin**

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Date: Friday, January 08, 2021		Sheet 10 of 13



P13:DC-DC
 AVS_FB << AVS_FB

VDD : 1.1V
 MCI_AVDD12D : 1.2V
 PLL_AVDD18 : 1.8V
 SRD1_AVDD18 : 1.8V
 SRD2_AVDD18 : 1.8V
 USB_AVDD18 : 1.8V
 VDDO_GIO : 1.8V
 VDDO_JIO : 1.8V
 VDDO_PIO : 1.8V
 VDDO_MMC : 3.3V
 VDDO_SD : 3.3V
 USB_AVDD33 : 3.3V
 VDDO_M : 1.8V



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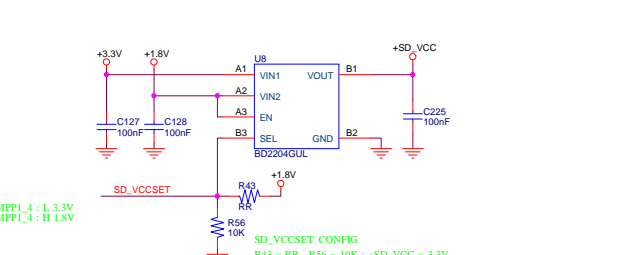
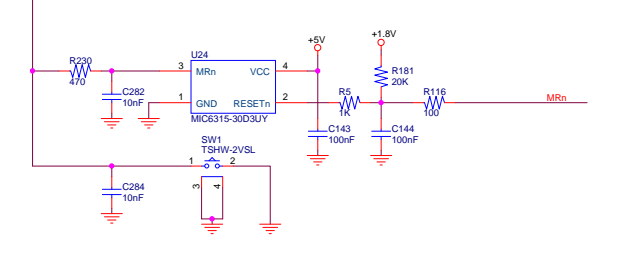
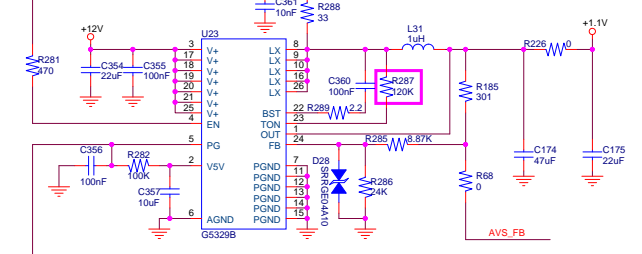
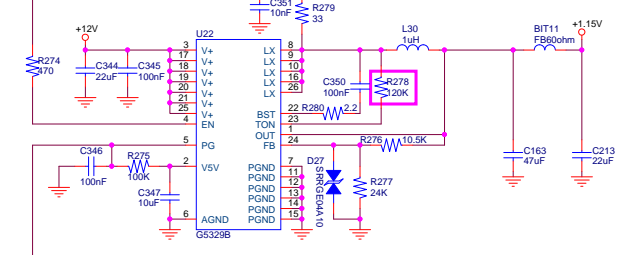
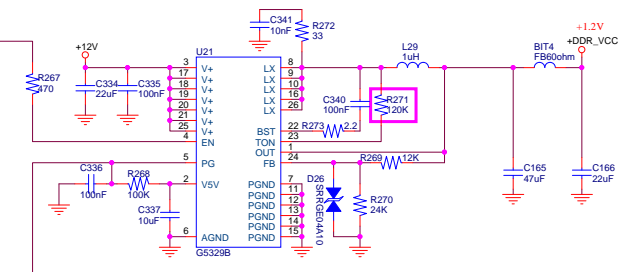
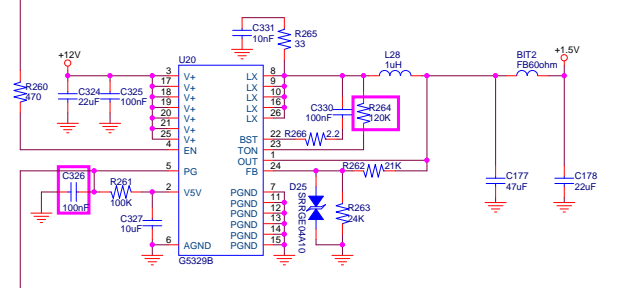
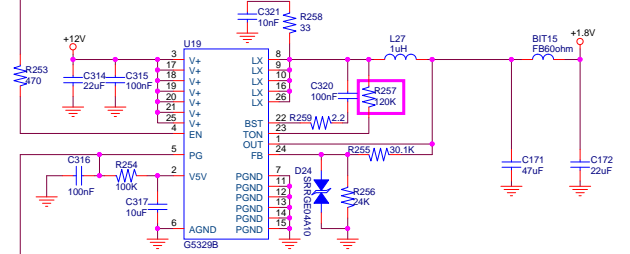
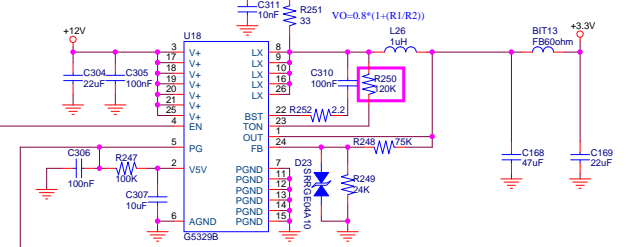
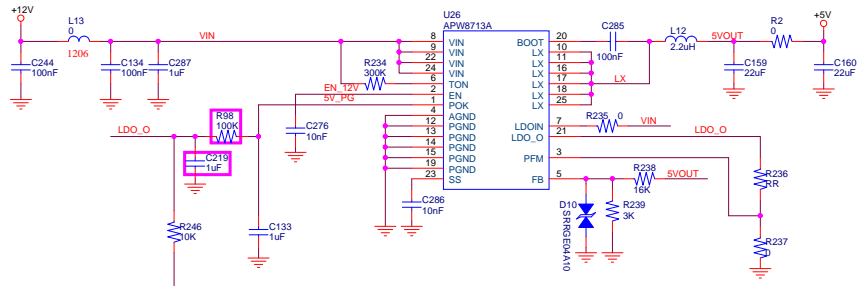
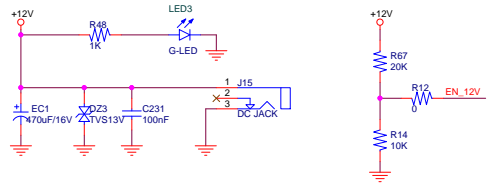
Title: **ESPRESSObin**

Size: A4	Document Number: 12-POWER	Rev: V7-3-3
Date: Wednesday, December 30, 2020 12 of 13		

P4: JTAG
MRn ← MRn

P6: GPIO
SD_VCCSET ← SD_VCCSET

P12: POWER
AVS_FB ← AVS_FB



MPPL4 : L 1.3V
MPPL4 : H 1.8V

SD_VCCSET CONFIG
R43 = RR, R56 = 10K : +SD_VCC = 3.3V
R43 = 10K, R56 = RR : +SD_VCC = 1.8V